National Institute of Technology Meghalaya

The National Institute of Technology (NIT) Meghalaya is one among the 31 NITs in India established under the NIT Act 2007 (Amended 2012) of the Parliament of India as Institutes of National Importance with full funding support from the Ministry of Human Resource Development, Government of India.

A Centre of Excellence vibrant with academic activities and bubbling with youthful creative energy, making significant contribution to the World of Knowledge and Technology and to the Development of the State, the Region and the Nation. NIT Meghalaya shall closely interact with the stake holders, the society, the governments, the NGOs and shall strive to work for the betterment of the state and the region.

Department of Electronics & Communication Engineering

Department of Electronics and Communication Engineering (ECE) was established in 2010 with the inception of National Institute of Technology Meghalaya. The department offers B. Tech Programme with an intake capacity of thirty & M. Tech Programme with an intake capacity of twenty in Electronics and Communication Engineering and Ph.D. program in various specialized areas of Electronics and Communication Engineering. The major research areas of the department include High Speed and Low Power VLSI, Computer Arithmetic, Wireless Sensor Networks, Cognitive Radio, Antenna Design and Signal Processing.

Organizing Commitee

Patron:

Prof. B. B. Biswal, Director, NIT Meghalaya

Convenor:

Dr. Anup Dandapat, Associate Professor,
Department of ECE, NIT Meghalaya

Resource Persons:

Prof. I. Sengupta, IIT Kharagpur

Dr. Anup Dandapat, NIT Meghalaya

Lab Assists:

Mr. Telajala Venkata Mahendra, Mr. Sheikh Wasmir Hussain

Short Term Training Programme on

Digital Design and Analysis at Backend Level Using CADENCE

Sponsered by TEQIP-III & SERB-DST Project entitled ``Ultra Low Power Multi Array 64K X 16 Dual Bit Associative Memory with Partial Matching Capability"

The primary objective of the program is to familiarize the students/scholars/faculties with digital VLSI design flow, implementation and modeling. The program is focused on training the participants to the custom IC design, Layout Flow, Various analysis to verify the robustness of any digital design.

The 5 days program covers guest lectures by invited speaker from IIT and Hands on LAB

Course Structure

	Session 1	Session 2
Day 1	Basic VLSI Design	Schematic Capture and Analysis
Day 2	Low Power Adder Design & Issues	Layout Flow
Day 3	Code Converters, Design with Decoders and MUXs	Lecture by Prof. I. Sengupta
Day 4	Lecture by Prof. I. Sengupta	Basic Digital Circuit Design
Day 5	Low Power Design Issues	Memory Design

Target Participant

- B.Tech/ M.Tech Students
- B.Sc./ M.Sc. Students in relevant field
- PhD Scholars/ Faculties

REGISTER

Important Dates

- Program : 5th - 9th March 2018
- Registration Closes: 3rd March 2018

Registration Process

Registration can be made online by mentioning the candidate details in google form. No registration fee for attending this short term training programme.

Instructions:

- Visit ***www.nitm.ac.in***
- Registration link is available below. Participant need to fill the google form.
- Confirmation of registration will be notified via email.
- No hardcopy of the application form to be sent.

Accomodation & Fooding

- Accomodation will not be provided. Accomodation has to arrange by the participants..
- High Tea and lunch will be provided on program days.

Availability of Seats:

Maximum **30**
(On First Come First Serve Basis)

Contact Details

Dr. Anup Dandapat
Associate Professor & Convenor
Department of Electronics & Communication Engineering
National Institute of Technology Meghalaya
Bijni Complex, Laitumkhrah, Shillong
Shillong- 793003

Email: **anup.dandapat@nitm.ac.in**
Phone: **09485177019**