Patron

Prof. B. B Biswal, Director, NIT Meghalaya

Organizing Chair

Dr. Anup Dandapat, NIT Meghalaya SMDP Coordinator

Convenors

Dr. A. Dandapat, NIT Meghalaya, ECE Dept.

Dr. P. Rangababu, NIT Meghalaya, ECE Dept.

Members:

Faculties of ECE Dept NIT Meghalaya

Experts/Resource Persons

Expert from IITs and NITs.

Who Can Register?

Faculty members of the technical institutions, Research and PG scholars.

Important Dates

Last date of application received	**26th Sept, 2021**
Intimation of participation	**26th Sept, 2021**

How to Register

- Interested participants may apply through online registration in link https://forms.gle/JiwHDtkJenRrTeG36 on or before 26th Sept 2021.
- ***No registration fee*** will be charged from the participants.
- The number of participants is limited to 100.
- Participant's registration will be confirmed on first come first serve basis. Certificate will be issued to those participants who attend all the sessions online

Contact:

Dr. A. Dandapat, Department of Electronics and Communication Engineering, NIT Meghalaya, Shillong, Phone: +91 9485177019, Email: anup.dandapat@nitm.ac.in

One Week Online Refresher Course

on

"Recent Trends in VLSI Design"

27th Sept – 1st Oct, 2021

Sponsored by

Special Manpower Development Programme

Organized by

Department of Electronics and Communication Engineering

National Institute of Technology Meghalaya

Venue

National Institute of Technology Meghalaya,

Bijni Complex, Laitumkhrah, Shillong –793003

Course Objective

In the past two decades, CMOS technology has rapidly embraced the field of analog and digital integrated circuits, providing low-cost, low power, and high-performance solutions and rising to dominate the market. While silicon bipolar and III-V devices still find niche applications, only CMOS processes have emerged as a viable choice for the integration of today's complex mixed signal and SOC systems. There is a strong demand of manpower having thorough knowledge and hands on experiences in VLSI design using state of the art EDA tools. The course aims to pique interest in the VLSI design field by briefly covering device-to-circuit-level understanding, IC design approaches, and an overview of state-of-the-art low-power design techniques. This course invites budding researchers and faculty members to acquire an experience in this field.

About NIT Meghalaya

National Institute of Technology Meghalaya was established in the year 2010 as joint venture of Govt. of India and Govt. of Meghalaya with granted permanent campus of around 450 acres at Shora Cherrapunjee. The institute is functioning in its temporary campus at Shillong in East Khasi Hills district of Meghalaya and is about 2 Kms from the main bus stand of Shillong on Police bazaar – Laitumkhrah roadway. The city of Shillong is well connected with rest of the country by road. The nearest railway station is at Guwahati (Assam), at a distance of 90 Kms from Shillong. The nearest airport is within city (15 Kms). The place has healthy climate with temperature ranging from 7°c to 16°c during December and is at an altitude of 1520 meters.

The Department of Electronics and Communication Engineering was established in the year 2010. The Department offers B. Tech, M. Tech, and Ph.D. programmes. The department is well equipped with laboratories, computers, latest simulation softwares and our students are exposed to recent technologies and techniques. The department has well experienced and dedicated faculty members with different research specializations in Microelectronics, VLSI Design and Embedded Systems, Communication and Digital Processing and RF Design.

Program Contents

- Semiconductor Device to Circuit level understanding
- Digital IC Design
- Challenges in IC Design
- Low Power Design Techniques
- Memory Design

National Institute of Technology Meghalaya, Bijni Complex, Shillong-793003

Course Schedule

Date	04:00 PM to 05:00 PM	05:00 PM to 06:00 PM
27.09.2021 (Monday)	Registration and Inauguration	**Session 1** Fundamentals of Semiconductor Devices/ MOS Fundamentals ***Prof. Srimanta Baishya, NIT Silchar***
28.09.2021 (Tuesday)	**Session 2a** VLSI Physical Design ***Prof. Indranil Sengupta, IIT Kharagpur***	**Session 2b** VLSI Physical Design ***Prof. Indranil Sengupta, IIT Kharagpur***
29.09.2021 (Wednesday)	**Session 3a** Low Power Design ***Dr. Anup Dandapat, NIT Meghalaya***	**Session 3b** Overview of MEMS and Pressure Sensors ***Dr. Pradeep Rathore, NIT Meghalaya***
30.09.2021 (Thursday)	**Session 4a** Reversible Computational Arithmetic Circuits ***Dr. Prabir Kumar Saha, NIT Meghalaya***	**Session 4b** Stream Architecture on FPGA ***Dr. P. Rangababu, NIT Meghalaya***
01.10.2021 (Friday)	**Session 5** Architectural Synthesis of VLSI Circuits ***Dr. Shubhajit Roy Chowdhury, IIT Mandi***	Valedictory Session and Certificate Distribution

NIT Meghalaya