	National Institute of Technology Meghalaya An Institute of National Importance	**CURRICULUM**

Programme	**Master of Technology in VLSI and Embedded Systems**	Year of Regulation	**2018-19**
Department	**Electronics and Communication Engineering**	Semester	**II**

Course Code	Course Name	Credit Structure				Marks Distribution		
		L	T	P	C	Continuous Evaluation	VIVA	Total
EC 568	**Low Power VLSI Design Lab**	**0**	**0**	**2**	**1**	**70**	**30**	**100**

Course Objectives		Course Outcomes		
	Learn how to make comparative design analysis		CO1	Able to learn the CADANCE EDA tool
	Learn to use ADE for different parametric use		CO2	Able to design different full adders
	Learn to make complex designs		CO3	Able to make comparative analysis of different designs
	Learn to make analysis for different bit combinations and for other parametric value		CO4	Able to analyze delay, power and other parameters of designs

No.	COs	Mapping with Program Outcomes (POs)												Mapping with PSOs			
		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3	PSO4
1	CO1	**3**	**3**	**0**	**1**	**0**	**0**	**0**	**0**	**2**	**0**	**0**	**0**	**3**	**0**	**0**	**3**
2	CO2	**3**	**3**	**3**	**1**	**0**	**0**	**0**	**0**	**2**	**0**	**0**	**0**	**2**	**0**	**0**	**2**
3	CO3	**2**	**3**	**3**	**1**	**2**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**2**	**3**	**3**	**2**

SYLLABUS

No.	Content	Hours	COs
	1. Design 3 different full adders and measure power and delay for all possible combinations. 2. Design a NAND based full adder and measures power and delay for all possible combinations. 3. Design a NOR based full adder and measures power and delay for all possible combinations. 4. Design a 4-bit binary comparator and make complete analysis.	24	CO1 CO2 CO3 CO4
	Total Hours	24	

Essential Readings

1. K. Roy and S. C. Prasad, Low Power CMOS VLSI Circuit Design, John Wiley and Sons, 3rd Edition, 2009.
2. Jan Rabaey, Low Power Design Essentials, Springer Publications, 1st Edition, 2009.
3. Chandrakasan and R. Brodersen, Low-Power CMOS Design, IEEE Press, 1st Edition, 1995.

Supplementary Readings

1. Chandrakasan, Bowhill, and Fox, Design of High-Performance Microprocessors, IEEE Press, 1st Edition, 2000.
2. G. Yeap, Practical Low Power Digital VLSI Design, Springer Publications, 1st Edition, 1995.