

|  | | National Institute of Technology Meghalaya An Institute of National Importance | | | | | | | | | | | CURRICULUM | | | | | | |
|---|--|--|----------|---|----------|-----------------------|-----------|------------|-----|-----|------|--------------------|-------------------|--------------------|------|------------------|------|--|--|
| Programme | | Master of Technology in VLSI and Embedded Systems | | | | | | | | | | Year of Regulation | | | | 2018-2019 | | | |
| Department | | Electronics and Communication Engineering | | | | | | | | | | Semester | | | | I | | | |
| Course Code | Course Name | Credit Structure | | | | | | | | | | | | Marks Distribution | | | | | |
| | | L | T | P | C | Continuous Evaluation | VIVA | Total | | | | | | | | | | | |
| EC 563 | VLSI Signal Processing Lab | 0 | 0 | 2 | 1 | 70 | 30 | 100 | | | | | | | | | | | |
| Course Objectives | To study high level architectures of hardware specific systems | Course Outcomes | CO1 | Describe the hardware description language, FPGA design concept | | | | | | | | | | | | | | | |
| | To understand concept of digital signal processor architecture | | CO2 | Understand architectural issues of digital signal processors | | | | | | | | | | | | | | | |
| | To develop the subsystem for Digital signal processors | | CO3 | Familiarize discrete Fourier transformation processor in FPGA | | | | | | | | | | | | | | | |
| | To understand the convolution processors | | | | | | | | | | | | | | | | | | |
| | To understand the concept filter design techniques in VLSI | | | | | | | | | | | | | | | | | | |
| No. | COs | Mapping with Program Outcomes (POs) | | | | | | | | | | | | Mapping with PSOs | | | | | |
| | | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 | PSO3 | PSO4 | | |
| 1 | CO1 | 0 | 0 | 0 | 1 | 1 | 1 | 3 | 0 | 0 | 0 | 0 | 0 | 0 | 3 | 0 | 3 | | |
| 2 | CO2 | 0 | 0 | 3 | 2 | 1 | 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 2 | 2 | | |
| 3 | CO3 | 0 | 0 | 0 | 0 | 2 | 2 | 0 | 3 | 0 | 0 | 0 | 0 | 0 | 0 | 3 | 2 | | |
| SYLLABUS | | | | | | | | | | | | | | | | | | | |
| No. | Content | | | | | | | | | | | | | Hours | COs | | | | |
| I | Fixed and Floating point number systems and its implementation in Hardware description languages | | | | | | | | | | | | | 06 | CO1 | | | | |
| II | Implementation of Signal Processing Algorithm in FPGA | | | | | | | | | | | | | 08 | CO2 | | | | |
| III | Implementation of Digital Filter in FPGA | | | | | | | | | | | | | 08 | CO3 | | | | |
| Total Hours | | | | | | | | | | | | | 22 | | | | | | |
| Essential Readings | | | | | | | | | | | | | | | | | | | |
| 1. K. K. Parhi, VLSI Digital Signal Processing Systems, Design and Implementation , John Wiley, 1999 | | | | | | | | | | | | | | | | | | | |
| 2. U. Meyer-Baese, Digital Signal processing with Field Programmable Arrays, Springer, 3rd edition 2007. | | | | | | | | | | | | | | | | | | | |
| 3. S. Ramachandran, Digital VLSI systems design. Springer, 2007. | | | | | | | | | | | | | | | | | | | |
| Supplementary Readings | | | | | | | | | | | | | | | | | | | |
| 4. V. K. Madiseti, VLSI Digital Signal Processors: An Introduction to Rapid Prototyping and Design Synthesis, IEEE Press, 1995. | | | | | | | | | | | | | | | | | | | |
| 5. S. Y. Kung, and H. J. Whitehouse, VLSI and Modern Signal Processing, Prentice Hall, 1985. | | | | | | | | | | | | | | | | | | | |
| 6. Chan, K. Pak and S.Mourad, Digital system design using field programmable gate arrays, Prentice-Hall, Inc, 1st edition 1994. | | | | | | | | | | | | | | | | | | | |