

		National Institute of Technology Meghalaya An Institute of National Importance												CURRICULUM					
Programme		Master of Technology in VLSI and Embedded Systems										Year of Regulation				2018-19			
Department		Electronics and Communication Engineering										Semester				II			
Course Code	Course Name	Credit Structure				Marks Distribution													
		L	T	P	C	Continuous Evaluation	VIVA	Total											
EC 556	VLSI Design Lab	0	0	2	1	70	30	100											
Course Objectives	Simulate the circuits for algorithms	Course Outcomes	CO1	Able to perform simulation, synthesis, verification of circuit															
	Perform Synthesize and verify the functionalities		CO2	Able to realize the chip from a circuit using Cadence EDA tools															
	Test the circuits with various faults		CO3	Able to use EDA tools for fabrication steps															
	Realize RTL to GDS to a circuit																		
	Use EDA tools for fabrication of IC																		
No.	COs	Mapping with Program Outcomes (POs)												Mapping with PSOs					
		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3	PSO4		
1	CO1	3	1	3	1	0	0	0	0	3	3	0	0	3	3	0			
2	CO2	1	3	3	3	0	0	0	0	2	0	3	0	2	2	0			
3	CO3	2	3	2	1	2	0	0	0	0	1	1	0	2	2	0			
SYLLABUS																			
No.	Content													Hours	COs				
I	1) Algorithm Basics Various algorithms for different applications like computer vision, digital signal processing etc 2) Architecture Design The goals of architecture design, the architectural solution space, dedicated VLSI architectures and how to design them, Equivalence transforms for combinational computations, Options for temporary storage of data, Equivalence transforms for non-recursive computations, Equivalence transforms for recursive computations, Generalizations of the transform approach. 3) Circuit Modelling A discrete replacement for electrical signals, an event-driven scheme of execution, Facilities for model parameterization, Key concepts and constructs of system Verilog, Automatic circuit synthesis from hdl models and its design 4) Parametric analysis on Layout Timing analysis, Fault analysis (Stuck at 1 or 0), Power dissipation analysis, Crosstalk and Interference analysis, Area Optimization Algorithms.													24	CO1 CO2 CO3				
Total Hours													24						
Essential Readings																			
1. S.M.Sze, "VLSI Technology", McGraw Hill, 2003																			
2. M. H. Rashid, "Introduction to PSpice using OrCAD for circuits and electronics", Prentice Hall, 2004																			
3. Erik Brunvand, "Digital VLSI Chip Design with Cadence and Synopsys CAD Tools", Pearson, 2010																			
Supplementary Readings																			
1. William I Fletcher, "An Engineering Approach to Digital Design", Prentice Hall, 2006																			
2. James E. Palmer, David E. Perlman, "Introduction to Digital Systems", Tata McGraw Hill, 2006																			
3. M,D,Ciletti, "Modeling, Synthesis and Rapid Prototyping with the Verilog HDL", Prentice Hall, 2006																			
4. Steven M. Rubin, "Computer Aids for VLSI Design", http://www.rulabinsky.com/cavd (free online book), 1997																			