	National Institute of Technology Meghalaya An Institute of National Importance	**CURRICULUM**

Programme	**M.Tech/Ph.D**	Year of Regulation	**2021**
Department	**Electronics and Communication Engineering**	Semester	**II**

Course Code	Course Name	Credit Structure				Marks Distribution			
		L	T	P	C	INT	MID	END	Total
EC 542	**Digital IC Design**	**3**	**0**	**0**	**3**	**50**	**50**	**100**	**200**

Course Objectives		Course Outcomes		
	Understand Various Design of ICs paradigms		CO1	Able to design of digital ICS
	Analyse the effect of various RC Delay Effects		CO2	Able to detect the effects of RC delays in ICs
	Study various timing effects of Various circuits		CO3	Able to identify and correct timing faults in a circuit
	Design arithmetic Sequential and memory blocks		CO4	Able to implement large scale digital systems in cadence

No.	COs	Mapping with Program Outcomes (POs)												Mapping with PSOs			
		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3	PSO 4
1	CO1	2	1	2	1	1	0	0	0	0	0	0	0	1	1	1	0
2	CO2	1	2	2	2	0	0	0	0	0	0	0	1	**1**	1	1	0
3	CO3	1	2	2	1	2	0	0	0	0	0	0	2	2	1	1	0
4	CO4	1	2	1	1	2	0	0	0	0	0	0	2	2	2	2	0

SYLLABUS

No.	Content	Hours	COs
I	**Implementation Strategies for Digital ICs** Introduction, From Custom to Semicustom and Structured Array Design Approaches, Custom Circuit Design, Cell-Based Design Methodology, Standard Cell, Compiled Cells, Macrocells, Megacells and Intellectual Property, Semi-Custom Design Flow, Array-Based Implementation Approaches, Pre-diffused (or Mask-Programmable) Arrays, Pre-wired Arrays, Perspective—The Implementation Platform of the Future	10	CO1
II	**The Wire** Introduction, A First Glance, Interconnect Parameters — Capacitance, Resistance, and Inductance, Electrical Wire Models, SPICE Wire Models.	5	CO1 CO2
III	**Coping with Interconnect** Introduction, Capacitive Parasitics, Capacitance and Reliability—Cross Talk, Capacitance and Performance in CMOS, Resistive Parasitics, Resistance and Reliability—Ohmic Voltage Drop, Electromigration, Resistance and Performance—RC Delay	5	CO2
IV	**Timing Issues in Digital Circuits** Introduction, Timing Classification of Digital Systems, Synchronous Interconnect, Mesochronous interconnect, Plesiochronous Interconnect, Asynchronous Interconnect, Synchronous Design — An In-depth Perspective, Synchronous Timing Basics, Sources of Skew and Jitter, Clock-Distribution Techniques, Synchronizers and Arbiters, Synchronizers—Concept and Implementation, Arbiters, Clock Synthesis and Synchronization Using a Phase-Locked Loop, Basic Concept, Building Blocks of a PLL	8	CO3
V	**Designing Arithmetic Building Blocks** Introduction, Datapaths in Digital Processor Architectures, The Adder, The Binary Adder: Definitions, The Full Adder: Circuit Design Considerations, The Binary Adder: Logic Design Considerations, The Multiplier, The Multiplier: Definitions, Partial-Product Generation, Partial Product Accumulation, Final Addition, Multiplier Summary, The Shifter, Barrel Shifter, Logarithmic Shifter	5	CO4
VI	**Designing Memory and Array Structures** Introduction, Memory Classification, Memory Architectures and Building Blocks, The Memory Core, Read-Only Memories, Nonvolatile Read-Write Memories, Read-Write Memories (RAM), Contents-Addressable or Associative Memory (CAM), Memory Peripheral Circuitry, The Address Decoders, Sense Amplifiers, Voltage References, Drivers/Buffers, Timing and Control	5	CO4
	Total Hours	38	

Essential Readings

1. Jan M. Rabaey Anantha Chandrakasan, & Borivoje Nikolic, “Digital Integrated Circuits – A design perspective”, Prentice-Hall 2nd Edition 2016
2. S. M. Kang & Y. Leblebici, “CMOS Digital Integrated Circuits”, McGraw Hill.3rd Edition 2002
3. Jackson & Hodges, “Analysis and Design of Digital Integrated circuits”. Tata McGraw- Hill 3rd Edition 2003

Supplementary Readings

1. Ken Martin, “Digital Integrated Circuit Design”, Oxford Publications 1st Edition 2004
2. Sedra and Smith, “Microelectronic Circuits”, Oxford Publications 7th Edition 2017