Programme	**M.Tech/Ph.D**				Year of Regulation		**2021**
Department	**Electronics and Communication Engineering**				Semester		**II**

Course Code	Course Name	Credit Structure				Marks Distribution			
		L	T	P	C	INT	MID	END	Total
EC 538	**Digital System Design**	**3**	**0**	**0**	**3**	**50**	**50**	**100**	**200**

Course Objectives	Introduce VHDL language Semantics	Course Outcomes	CO1	Able to understand and VHDL language capabilities
	Design LSI, MSI, VLSI circuits using HDL		CO2	Able to design various Electronics Circuits using HDL
	Design Various controllers using State machines		CO3	Able to design and energy efficient and high-performance digital systems
	Implement the circuits on FPGAs and ASICs		CO4	Able to implement the circuits in FPGAs

No.	COs	Mapping with Program Outcomes (POs)												Mapping with PSOs			
		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3	PSO4
1	CO1	1	2	2	0	1	0	0	0	0	0	0	0	2	1	1	0
2	CO2	1	1	2	2	0	0	0	0	0	0	0	1	2	1	2	0
3	CO3	1	2	2	2	2	0	0	0	0	0	0	1	1	1	1	0
4	CO4	1	1	1	2	2	0	0	0	0	0	0	1	1	1	2	0

SYLLABUS			
No.	Content	Hours	COs
I	**Introduction to VHDL** Computer-Aided Design / Hardware Description Languages / VHDL Description of Combinational Circuits / VHDL Modules / Sequential Statements and VHDL Processes / Modelling Flip-Flops Using VHDL Processes / Processes Using Wait Statements / Two Types of VHDL Delays: Transport and Inertial Delays / Compilation, Simulation, and Synthesis of VHDL Code / VHDL Data Types and Operators / Simple Synthesis Examples / VHDL Models for Multiplexers / VHDL Libraries / Modelling Registers and Counters Using VHDL Processes / Behavioural and Structural VHDL / Variables, Signals, and Constants / Arrays / Loops in VHDL / Assert and Report Statements	10	CO1
II	**Introduction to Programmable Logic Devices** Brief Overview of Programmable Logic Devices / Simple Programmable Logic Devices (SPLDs) / Complex Programmable Logic Devices (CPLDs) / Field-Programmable Gate Arrays (FPGAs) Design Examples: BCD to 7-Segment Display Decoder / A BCD Adder / 32-Bit Adders / Traffic Light Controller / State Graphs for Control Circuits / Scoreboard and Controller / Synchronization and Debouncing / A Shift-and-Add Multiplier / Array Multiplier / A Signed Integer/Fraction Multiplier / Keypad Scanner / Binary Dividers	12	CO2
III	**State Machine** State Machine, Moore Machine, Melay Machine	4	CO2 CO3
IV	**Designing with Field Programmable Gate Arrays** Implementing Functions in FPGAs / Implementing Functions Using Shannon's Decomposition / Carry Chains in FPGAs / Cascade Chains in FPGAs / Examples of Logic Blocks in Commercial FPGAs / Dedicated Memory in FPGAs / Dedicated Multipliers in FPGAs / Cost of Programmability / FPGAs and One-Hot State Assignment / FPGA Capacity: Maximum Gates Versus Usable Gates / Design Translation (Synthesis) / Mapping, Placement, and Routing.	10	CO3 CO4
	Total Hours	36	

Essential Readings

1. Charles Roth, Lizy Kurian John, "Principles of Digital System Design using VHDL", Cengage Learning. 1st Edition, 2008

2. John F. Wakerly, "Digital Design Principles and Practices", Pearson Education.4th Edition, 2008

3. Charles Roth, "Digital Systems Design using VHDL" , Cengage Learning.3rd Edition 2017

Supplementary Readings

1. Michael Ciletti, "Advanced Digital Design using Verilog HDL", Prentice Hall Publications. 2nd Edition 2017

2. P.K.Chan & S. Mourad, "Digital Design Using Field Programmable Gate Array", Prentice Hall.2009