	National Institute of Technology Meghalaya An Institute of National Importance	**CURRICULUM**

Programme	**Master of Technology in VLSI and Embedded Systems**	Year of Regulation	**2018-19**
Department	**Electronics and Communication Engineering**	Semester	**II**

Course Code	Course Name	Credit Structure				Marks Distribution			
		L	T	P	C	INT	MID	END	Total
EC 510	**MEMORY TECHNOLOGIES AND TESTING**	**3**	**0**	**0**	**3**	**50**	**50**	**100**	**200**

Course Objectives		Course Outcomes		
	Basics of MOS devices		CO1	Able to understand basics of MOS Devices.
	Basics of Volatile and non-volatile Memories		CO2	Able to learn Volatile and non-volatile Memories.
	Fundamentals of silicon-based memories		CO3	Able to learn silicon-based memories.
	Memory Design and testing		CO4	Able to learn Memory fault modelling and testing

No.	COs	Mapping with Program Outcomes (POs)												Mapping with PSOs			
		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3	PSO4
1	CO1	**3**	**3**	**0**	**1**	**0**	**0**	**0**	**0**	**2**	**0**	**0**	**0**	**3**	**0**	**0**	**3**
2	CO2	**3**	**3**	**3**	**1**	**0**	**0**	**0**	**0**	**2**	**0**	**0**	**0**	**2**	**0**	**0**	**2**
3	CO3	**2**	**3**	**3**	**1**	**2**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**2**	**3**	**3**	**2**
4	CO4	**2**	**2**	**3**	**0**	**2**	**2**	**3**	**0**	**2**	**0**	**0**	**1**	**2**	**3**	**2**	**2**

SYLLABUS

No.	Content	Hours	COs
I	Review of MOS Band diagrams; threshold voltage; body bias effect; drain current and gate current characteristics; subthreshold slope; hot electron effect; various leakages in a MOSFET; tunneling phenomenon; direct tunneling; direct band to band tunneling; SOI MOSFET; PDSOI; FDSOI; classification of memories.	5	CO1
II	Volatile memories SRAM functionality: architecture, timing diagrams, performance and timing specifications; low voltage SRAMs; SOI SRAMs; content addressable memories (CAMs); 3-transistor DRAM; 1 transistor DRAM: functionality, architecture, timing diagrams, performance and timing specifications; sense amplifier; word line driver; leakage mechanisms in a DRAM; retention; retention time calculations.	7	CO2
III	Nonvolatile memories FLASH memories; floating gate theory; structure and working of a SONOS cell; structure and working FLOTOX memories; multi-level flash memories; NOR based flash memories; NAND based flash memories.	6	CO2
IV	Non silicon based memories PCRAM; MRAM; FeRAM; array device considerations for non-silicon based memories.	7	CO3
V	Memory fault modeling and testing RAM fault modeling; RAM electrical testing; RAM pseudo random testing; megabit DRAM testing; nonvolatile memory modeling and testing; IDDQ fault modeling and testing; application specific memory testing.	6	CO4
VI	Memory design for testability and fault tolerance General design for testability techniques; RAM built-in self-test (BIST); embedded memory DFT and BIST techniques; advanced BIST and built-in self-repair architectures; DFT and BIST for ROMs; memory error-detection and correction techniques; memory fault-tolerance designs.	5	CO4
Total Hours		36	

Essential Readings

1. A. K. Sharma, Semiconductor Memories: Technology, Testing and Reliability, Wiley IEEE Press, 1997.
2. K. Sharma, Advanced Semiconductor Memories: Architectures, Design and Applications, Wiley- IEEE Press, 2003.
3. W. D. Brown, and Joe Brewer, Nonvolatile Semiconductor Memory Technology: A Comprehensive Guide to Understanding and Using NVSM Devices, Wiley-IEEE Press, 1997.

Supplementary Readings

1. J. Brewer, Nonvolatile Memory Technologies with Emphasis on Flash: A Comprehensive Guide to Understanding and Using Flash Memory Devices, Manzur Gill, Wiley-IEEE Press, 2008.
2. J.-P. Colinge, FinFETs and Other Multi-Gate Transistors Springer, 2008.
3. Y. Taur and T.H. Ning, Fundamentals of Modern VLSI Devices, Cambridge University Press, 1998.