



National Institute of Technology Meghalaya
An Institute of National Importance

CURRICULUM

Programme		Master of Technology in VLSI and Embedded Systems											Year of Regulation		2018-19			
Department		Electronics and Communication Engineering											Semester		I			
Course Code	Course Name	Credit Structure				Marks Distribution												
		L	T	P	C	INT	MID	END	Total									
EC 503	Digital VLSI Circuits	3	0	0	3	50	50	100	200									
Course Objectives	Preliminaries on MOS Devices	Course Outcomes	CO1	Able to understand basic design structure of MOS														
	Fundamentals of Inverter Design and analysis		CO2	Able to design and Analyze CMOS inverter VTC														
	Basic combinational CMOS Designs		CO3	Able to design CMOS combinational and sequential circuits														
	Basic sequential CMOS Designs		CO4	Able to design CMOS sub systems														
No.	COs	Mapping with Program Outcomes (POs)												Mapping with PSOs				
		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3	PSO4	
1	CO1	3	3	0	1	0	0	0	0	2	0	0	0	3	0	0	3	
2	CO2	3	3	3	1	0	0	0	0	2	0	0	0	2	0	0	2	
3	CO3	2	3	3	1	2	0	0	0	0	0	0	0	2	3	3	2	
4	CO4	2	2	3	0	2	2	3	0	2	0	0	1	2	3	2	2	
SYLLABUS																		
No.	Content													Hours	COs			
I	Introduction to MOS Device: First Glance at the MOS device MOS Transistor under static conditions, threshold voltage, channel length modulation, velocity saturation, hot carrier effect, sub threshold conduction, MOS structure capacitance.													5	CO1			
II	MOS Transistor Device Modeling: Basic concepts-LEVEL1-LEVEL2-LEVEL3 modeling technique-various model comparison. Static CMOS inverter, performance of CMOS inverter, propagation delay sizing inverter for performance.													6	CO1 CO2			
III	CMOS combinational logic design: Static CMOS designs, complementary CMOS design, power consumption in CMOS logic gates, design techniques to reduce switching activity, pass transistor logic, differential pass transistor logic, dynamic CMOS design, Domino CMOS logic, NPCMOS-logic style.													8	CO3			
IV	CMOS sequential logic design: Timing metrics for sequential circuit, multiplexer based latches, master slave edge triggered registers, non-ideal clock signals, low voltage static latches, static SR flip flop, Dynamic latches and registers, Dual edge registers, bi-stable sequential circuit-Schmitt trigger-mono stable –Astable -sequential circuit - choosing a clocking strategy.													8	CO3			
V	CMOS subsystem design: Addition/Subtraction, Comparators, Zero/One Detectors, Binary Counters, ALUs, Multiplication, Shifters, memory elements, finite-State Machines.													8	CO4			
Total Hours													35					
Essential Readings																		
1. R. Jan, Chandrakasan, and A. Nikolic, Digital Integrated Circuits: A Design Perspective, Pearson Education 2nd edition 2016.																		
2. N. H.E Weste and K. Eshraghian, Principles of CMOS VLSI Design, Addition Wesley, 2nd edition 1993.																		
Supplementary Readings																		
1. S-M. Kang and Y. Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, Tata McGraw-Hill, 3 rd edition 2002.																		