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| | **National Institute of Technology Meghalaya**<br>An Institute of National Importance | **CURRICULUM** |

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|---|---|---|---|
| Programme | **Master of Technology in VLSI and Embedded Systems** | Year of Regulation | **2018-19** |
| Department | **Electronics and Communication Engineering** | Semester | **I** |

| Course Code | Course Name | Credit Structure | | | | Marks Distribution | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | L | T | P | C | INT | MID | END | Total |
| **EC 501** | **Embedded Systems & Architectures** | **3** | **0** | **0** | **3** | **50** | **50** | **100** | **200** |

| Course Objectives | | Course Outcomes | | |
|---|---|---|---|---|
| | To understand ARM processor, bus architecture, memory map and I/O devices | | CO1 | Ability to identify ARM Processor architecture functionality and its operation |
| | To develop programs for ARM processor through various levels of high level and assemble programming. | | CO2 | Able to gain knowledge on ARM microprocessor and higher-end processor architectures, GPIO, Counters & Timers, Serial Data Input/ Output and Interrupts. Design example for interfacing Keys, LED/LCD Displays, ADC & DAC |
| | To learn the interfacing services of input/output peripherals of the processor | | CO3 | Able to demonstrate knowledge through programming in assembly and high-level programming languages |
| | To develop small applications by utilizing the ARM/higher end processor on the embedded platform | | CO4 | Abe to apply the knowledge to realize embedded applications |

| No. | COs | Mapping with Program Outcomes (POs) | | | | | | | | | | | | Mapping with PSOs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 | PSO3 | |
| 1 | CO1 | **2** | **3** | **2** | **1** | **0** | **3** | **0** | **0** | **2** | **0** | **0** | **0** | **3** | **0** | **3** | |
| 2 | CO2 | **3** | **2** | **0** | **1** | **0** | **0** | **0** | **0** | **2** | **0** | **0** | **0** | **2** | **0** | **2** | |
| 3 | CO3 | **2** | **3** | **3** | **1** | **2** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **2** | **3** | **0** | |
| 4 | CO4 | **2** | **2** | **3** | **0** | **2** | **2** | **3** | **0** | **2** | **0** | **0** | **1** | **0** | **3** | **2** | |

**SYLLABUS**

| No. | Content | Hours | COs |
|---|---|---|---|
| I | ARM Cortex-M3 processor:<br>Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces | 10 | CO1<br>CO3 |
| II | Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behaviour, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency. | 10 | CO3 |
| III | LPC 17xx microcontroller:<br>Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT | 9 | CO4 |
| IV | Programmable DSP (P-DSP) Processors:<br>Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations Code Composer Studio for application development for digital signal processing, On chip peripherals , Processor benchmarking | 8 | CO1<br>CO2 |
| | Total Hours | 37 | |

**Essential Readings**


1. Embedded Systems with ARM Cortex-M Microcontrollers in Assembly Language and C ,Third Edition, E-Man Press LLC, 2017
2. J. Yiu, The definitive guide to ARM Cortex-M3, Elsevier, 2nd edition 2009.
3. B. VenkatramaniandM. Bhaskar, Digital Signal Processors: Architecture, Programming and Applications,TataMcGraw Hill 2002.
4. S. Andrew N, S. Dominic, and W. Chris, ARM System Developer's Guide: Designing and Optimizing, Morgan Kaufman Publication, 2004.


**Supplementary Readings**


1. S. Furber, ARM System-on-Chip Architecture, Pearson Education, 2nd edition 2001
2. F. Vahid and T. Givargis, Embedded System Design, Wiley, 2001.
3. Technical references and user manuals on www.arm.com, NXP Semiconductor www.nxp.com and Texas Instruments www.ti.com.