National Institute of Technology Meghalaya

An Institute of National Importance

CURRICULUM

Programme	**Bachelor of Technology in Electronics and Communication Engineering**	Year of Regulation	**2018-19**
Department	**Electronics and Communication Engineering**	Semester	**VII**

Course Code	Course Name	Credit Structure				Marks Distribution			
		L	T	P	C	INT	MID	END	Total
EC 425	**CAD for VLSI Design**	**3**	**0**	**0**	**3**	**50**	**50**	**100**	**200**

Course Objectives		Course Outcomes		
	Understand the complete design methodology of VLSI automation		CO1	Understand of VLSI Design Automation.
	Design and synthesis the basic level circuits and High level synthesis circuits		CO2	Acquire knowledge about CAD tools used for VLSI design.
	Understand Algorithms for VLSI Design Automation		CO3	Able to understanding Algorithms for VLSI Design Automation.
			CO4	Able to gather knowledge of High Level Synthesis.
			CO5	Able to perform Timing Analysis on a circuits

No.	COs	Mapping with Program Outcomes (POs)												Mapping with PSOs			
		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3	PSO4
1	CO1	**2**	**2**	-	-	-	-	-	-	-	-	-	-	**3**	**1**	-	-
2	CO2	**2**	**3**	**2**	-	-	-	-	-	-	-	-	-	**3**	**1**	**2**	-
3	CO3	**2**	**3**	**2**	-	-	-	-	-	-	-	-	**2**	**2**	**1**	**2**	-
4	CO4	**2**	**2**	-	-	-	-	-	-	-	-	-	**2**	**2**	**1**	-	-

SYLLABUS

No.	Content	Hours	COs
I	VLSI design flow, CMOS based logic design, challenges, introduction and use in synthesis, modeling combinational and sequential logic, writing test benches. two-level and multilevel gate-level optimization, state assignment of finite state machines and timing	**12**	**CO1**
II	High-level synthesis: basic concepts, partitioning, scheduling, allocation and binding. Technology mapping. Testability issues: fault modeling and simulation, test generation, design for testability, built-in self-test. Testing SoC's. Basic concepts of verification	**12**	**CO2**
III	Physical design automation: review of MOS/CMOS fabrication technology. VLSI design styles: full custom, standard-cell, gate-array and FPGA. Physical design automation algorithms: floor-planning, placement, routing, compaction, design rule check, power and delay estimation, clock and power routing, etc. Special considerations for analog and mixed-signal designs.	**12**	**CO3**
	Total Hours	**36**	

Essential Readings

1. N.A. Sherwani, "Algorithms for VLSI physical design automation", Kluwer Academic Publishers, Ist edition, 1999
2. J. Bhasker, "Verilog VHDL synthesis: a practical primer", B S Publications Ist edition, 1998
3. M M. Sarrafzadeh and C.K. Wong, "An introduction to physical design", McGraw Hill, 1996
4. D.D. Gajski, N.D. Dutt, A.C. Wu and A.Y. Yin, "High-level synthesis: introduction to chip and system design", Kluwer Academic Publishers.Ist edition 1992

Supplementary Readings

1. M.J. Sebastian Smith and A. Wesley, "Application-specific integrated circuits", Addison-Wesley Pub, 2008
2. M.L. Bushnell and V.D. Agrawal, "Essentials of Electronic Testing", Kluwer Academic Publishers, 2000