	National Institute of Technology Meghalaya An Institute of National Importance	**CURRICULUM**

Programme	**Bachelor of Technology in Electronics and Communication Engineering**	Year of Regulation	**2018-19**
Department	**Electronics and Communication Engineering**	Semester	**VII**

Course Code	Course Name	Credit Structure				Marks Distribution			
		L	T	P	C	INT	MID	END	Total
EC 421	**VLSI Signal Processing**	**3**	**0**	**0**	**3**	**50**	**50**	**100**	**200**

Course Objectives		Course Outcomes		
	To study high level architectures of hardware specific systems		CO1	Describe the hardware description language, FPGA design concept
	To understand concept of digital signal processor architecture		CO2	Understand architectural issues of digital signal processors
	To develop the subsystem for Digital signal processors		CO3	Familiarize discrete Fourier transformation processor in FPGA
	To understand the convolution processors		CO4	Convolution architecture design in FPGA
	To understand the concept filter design techniques in VLSI		CO5	Filter design techniques w.r.t VLSI circuits
			CO6	

No.	COs	Mapping with Program Outcomes (POs)												Mapping with PSOs		
		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	CO1	-	-	**1**	**1**	**1**	**3**	-	-	-	-	-	-	**3**	-	**3**
2	CO2	-	**3**	**2**	**1**	**3**	-	-	-	-	-	-	-	-	**2**	**2**
3	CO3	-	-	-	**2**	**2**	-	**3**	-	-	-	-	-	-	**3**	**2**
4	CO4	-	**2**	**3**	-	-	-	-	-	-	-	-	-	**2**	**3**	**2**
5	CO5	-	-	-	**2**	**2**	-	**3**	-	-	-	-	-	**3**	**3**	**3**
6	CO6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

SYLLABUS

No.	Content	Hours	COs
I	**Introduction to Digital systems** Digital system design options and trade-offs, Design methodology and technology overview, High Level System Architecture and Specification, Behavioral modeling and simulation. Fixed and Floating point systems Hardware description languages, combinational and sequential design, state machine design, synthesis issues, test benches. Overview of FPGA architectures and technologies: FPGA Architectural options, granularity of function and wiring resources	**10**	**CO1**
II	**Architectural issues in DSP** Linear system theory, DFT, FFT, realization of digital filters. Data flow graph representation of DSP algorithm. Binary Adders, Binary multipliers, Multiply Accumulator (MAC) and Sum of Product (SOP). Pipelining and Parallel Processing, Retiming, Unfolding, Folding, Systolic, Distributed arithmetic, Cordic architecture design.	**12**	**CO2, CO3**
III	**Fast Convolution** Cook-Toom algorithm and modified Cook-Toom algorithm, Winograd algorithm, modified Winograd algorithm, Algorithmic strength reduction in filters and transforms, DCT and inverse DCT, parallel FIR filters and analysis of finite word length effects	**08**	**CO3, CO4, CO5**
IV	**Design of Low Power Filters** Scaling versus power consumption, power analysis, power reduction techniques, power estimation techniques, low power IIR filter design, Low power CMOS lattice IIR filter.	**08**	**CO4, CO5**
	Total Hours	**38**	

Essential Readings

1. K. K. Parhi, “VLSI Digital Signal Processing Systems, Design and Implementation”, John Wiley, 1st Edition, 1999.
2. U. Meyer-Baese, “Digital Signal processing with Field Programmable Arrays”, Springer, 3rd Edition 2007.

Supplementary Readings

1. S. Ramachandran, Digital VLSI systems design . Springer, 2007.
2. V. K. Madisetti, “VLSI Digital Signal Processors: An Introduction to Rapid Prototyping and Design Synthesis”, IEEE Press, 1st Edition, 1995.
3. S. Y. Kung, and H. J. Whitehouse, VLSI and Modern Signal Processing, Prentice Hall, 1st Edition, 1985.
4. Chan, K. Pak and S.Mourad, Digital system design using field programmable gate arrays, Prentice-Hall, Inc, 1st Edition 1994.