Programme	**Bachelor of Technology in Electronics and Communication Engineering**	Year of Regulation	**2018-2019**
Department	**Electronics and Communication Engineering**	Semester	**VII**

Course Code	Course Name	Credit Structure				Marks Distribution			
		L	T	P	C	INT	MID	END	Total
EC 411	**VLSI Design**	**3**	**0**	**0**	**3**	**50**	**50**	**100**	**200**

Course Objectives	To study the flow chart of ASICs and FPGAs	Course Outcomes	CO1	Describe the different phases of the design flow for digital ASICs
	To understand the Propagation delay and Power consumption of CMOS		CO2	Understand basic clocking issues
	To develop the subsystem for Digital VLSI circuits		CO3	Familiarize with CAD tool capabilities and limitations
	To understand the digital circuits With VHDL		CO4	Use automatic synthesis, placement and routing tools to implement a design
	To understand the concept of synthesize of digital circuits		CO5	Able to analyse and design of CMOS digital circuits
			CO6	

No.	COs	Mapping with Program Outcomes (POs)												Mapping with PSOs		
		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	CO1	2	-	1	1	1	-	-	-	-	-	-	-	3	-	3
2	CO2	-	3	2	1	-	-	-	-	-	-	-	-	-	2	2
3	CO3	-	-	3	2	2	-	-	-	-	-	-	-	2	3	2
4	CO4	-	2	3	-	-	-	-	-	-	-	-	-	2	3	2
5	CO5	-	-	3	2	2	-	-	-	-	-	-	-	3	3	3
6	CO6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

	SYLLABUS		
No.	Content	Hours	COs
I	**Introduction to VLSI design** Application specific Integrated circuits (ASICs) , VLSI Design Styles, VLSI Design Flow, Design Hierarchy, PLA, PAL, PLD and CPLD.	**04**	**CO1**
II	**Propagation delay & delay equations** Delay definition, Propagation delay of CMOS inverter chain, Delay equation: Switching resistance, input & output capacitance Delay sensitivity to channel length, width & gate-oxide thickness. Delay sensitivity to power supply, Delay sensitivity to parasitic resistance & capacitance, Calculation of interconnect delay, Elmore delay	**06**	**CO2**
III	**Power consumption in CMOS circuits** Dynamic/switching power, Static / Leakage power, Short circuit power	**04**	**CO2, CO3**
IV	**Sub System Design** Circuit techniques for low power design, Low voltage low power Adders, Low voltage low power Multipliers Low voltage low power ROM	**04**	**CO3, CO4**
V	**Digital modeling and simulation with VHDL** Introduction to VHDL, Basic Language Elements, Structural modeling, Data-flow modelling, Behavioral styles of modeling. Basic language elements. Entities, architecture specification and configurations. Syntax and Semantics of VHDL. Variable and signal types, arrays and attributes. Operators, expressions and signal assignments. Packages & Libraries. Component instantiation. Synthesis. Timing Simulation. Use of Procedures and functions, Examples of design using VHDL.	**06**	**CO1, CO2, CO3, CO4**
VI	**FPGA concept, architecture and programming** Introduction to ASICs and FPGAs; Fundamentals in digital IC design FPGA & CPLD Architectures; FPGA Programming Technologies; FPGA Logic Cell Structures; FPGA Programmable Interconnect and I/O Ports; FPGA Implementation of Combinational Circuits; FPGA Sequential Circuits; Timing Issues in FPGA Synchronous Circuits	**07**	**CO1, CO4**
VII	**Physical design automation (Placement, Floor Planning, Routing)** Basics of Layout: Design rule, Layout design of CMOS circuits, Circuit partitioning, Placement & routing algorithm, Design rule verification	**07**	**CO5**
	Total Hours	**38**	

Essential Readings

1. M. Sarrafzadeh and C. K. Wong, "An Introduction to VLSI Physical Design", McGraw Hill, 1st Edition, 1996

2. P. Ashenden, "Digital Design using VHDL", Elsevier, 1st Edition, 2007

Supplementary Readings

1. P.J Anderson, "The designer's guide to VHDL", Morgan Kaufman, 1st Edition, 2008

2. N.H.E. Weste, K. Haase, D. Harris, A. Banerjee, "CMOS VLSI Design: A circuits and Systems Perspective", Pearson Education, 4th Edition, 2011

3. W.Wolf , "FPGA System design", Pearson, 1st Edition, 2004

4. S. H. Gerez, "Algorithms for VLSI design automation", Wiley, 1st Edition, 1998