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| | **National Institute of Technology Meghalaya**<br>An Institute of National Importance | **CURRICULUM** |

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|---|---|---|---|
| Programme | **Bachelor of Technology in Electronics and Communication Engineering** | Year of Regulation | **2018-19** |
| Department | **Electronics and Communication Engineering** | Semester | **IV** |

| Course Code | Course Name | Credit Structure | | | | Marks Distribution | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | L | T | P | C | INT | MID | END | Total |
| **EC 224** | **Computer Architecture** | **3** | **0** | **0** | **3** | **50** | **50** | **100** | **200** |

| Course Objectives | Course Outcomes | | |
|---|---|---|---|
| To describe computer architecture concepts and mechanisms related to the design of modern processors, memories. | | CO1 | Ability to understand the basic structure of computer. |
| To apply this understanding to new computer architecture design problems within the context of balancing application requirements against technology constraints. | | CO2 | Ability to understand control unit operations. |
| To evaluate various design alternatives and make a compelling quantitative and/or qualitative argument for why one design is superior to the other approaches. | | CO3 | Ability to perform computer arithmetic operations. |
| | | CO4 | Ability to understand the concept of cache mapping techniques. |

| No. | COs | Mapping with Program Outcomes (POs) | | | | | | | | | | | | Mapping with PSOs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 | PSO3 | PSO4 |
| 1 | CO1 | **2** | **3** | **3** | **3** | **-** | **-** | **-** | **-** | **-** | **-** | **-** | **-** | **2** | **-** | **3** | **-** |
| 2 | CO2 | **2** | **3** | **2** | **2** | **-** | **-** | **-** | **-** | **-** | **-** | **-** | **-** | **3** | **-** | **3** | **-** |
| 3 | CO3 | **2** | **3** | **3** | **2** | **2** | **-** | **-** | **-** | **-** | **-** | **-** | **-** | **1** | **3** | **1** | **-** |
| 4 | CO4 | **2** | **3** | **2** | **2** | **2** | **2** | **-** | **-** | **-** | **-** | **-** | **-** | **2** | **2** | **-** | **-** |

**SYLLABUS**

| No. | Content | Hours | COs |
|---|---|---|---|
| I | **Fundamental Processors:**<br>Instruction set architecture; single-cycle, FSM, and pipelined processor microarchitecture; resolving structural, data, control, and name hazards; and analyzing processor performance. | **05** | **CO1** |
| II | **Processor Organization:**<br>Instruction set architecture- types, formats, addressing modes; Register set; Assembly language programming. Data path organization, Control unit design - Hardwired control, Microprogramming. CISC and RISC architecture, Instruction pipelining. | **08** | **CO2** |
| III | **Arithmetic and Logic unit:**<br>Computer arithmetic- Review of addition and subtraction; Multiplication- Booth's, Array; Division- Restoring and non-restoring; Floating-point arithmetic. | **10** | **CO2, CO3** |
| IV | **Fundamental Memories:**<br>Memory technology; direct-mapped vs. associative caches; write- through vs write-back caches; memory protection, translation, and virtualization; FSM and pipelined cache microarchitecture; analyzing memory performance; and integrating processors and memories. | **08** | **CO4** |
| V | **Advanced Memories:**<br>Advanced cache microarchitecture; memory synchronization, consistency, and coherence. | **05** | **CO3, CO4** |
| | Total Hours | **36** | |

**Essential Readings**


1. Hamacher, Vranesic, and Zaky, "Computer Organization", McGraw Hill, 5 th ed, 2002.
2. Mano M.M., "Computer System Architecture", PHI (EEE), 3 rd ed, 2016.


**Supplementary Readings**


1. Stallings, "Computer Organization and Architecture", PHI (EEE, 8 th ed, 2010.