	National Institute of Technology Meghalaya An Institute of National Importance	**CURRICULUM**

Programme	**Bachelor of Technology in Electronics and Communication Engineering**	Year of Regulation	**2018-19**
Department	**Electronics and Communication Engineering**	Semester	**III**

Course Code	Course Name	Credit Structure				Marks Distribution			
		L	T	P	C	INT	MID	END	Total
EC 203	**Digital Logic Design**	**3**	**1**	**0**	**4**	**50**	**50**	**100**	**200**

Course Objectives	To understand the principles of Boolean logic and optimize the circuits.	Course Outcomes	CO1	Able to understand the basic concepts of Boolean algebra and optimization of circuits.
	To develop the skills for modular Boolean, Arithmetic and Sequential circuits.		CO2	To design combinational and sequential circuits.
	To develop the student ability to design circuits using EDA tools		CO3	Able to predict and analyse the behaviour of synchronous and asynchronous circuits.
			CO4	To apply the CAD tools to realize digital circuits and behaviour

No.	COs	Mapping with Program Outcomes (POs)												Mapping with PSOs			
		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3	PSO4
1	CO1	**3**	**2**	**3**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**3**	**-**	**3**	**3**
2	CO2	**2**	**2**	**-**	**1**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**3**	**-**	**3**	**3**
3	CO3	**3**	**3**	**2**	**1**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**3**	**2**	**2**
4	CO4	**2**	**2**	**2**	**-**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**3**	**3**	**2**

SYLLABUS

No.	Content	Hours	COs
I	**Number Systems and Codes:** Addition, Subtraction, Multiplication and Division using Different Number Systems; Representation of Binary Number in Sign-Magnitude, Sign 1's Complement and Sign 2's Complement Notation; Rules for Addition and Subtraction with Complement Representation; BCD, EBCDIC, ASCII, Extended ASCII, Gray and other Codes. **Boolean Algebra and Switching Functions:** Basic Logic Operation and Logic Gates, Truth Table, Basic Postulates and Fundamental Theorems of Boolean Algebra, Standard Representations of Logic Functions- SOP and POS Forms, Simplification of Switching Functions-K-Map and Quine-Mc- Cluskey Tabular Methods, Synthesis of Combinational Logic Circuits.	**13**	**CO1**
II	**Combinational Logic Circuits Using MSI Integrated Circuits Programming:** Binary Parallel Adder, BCD Adder, Encoder Priority Encoder, Decoder, Multiplexer and Demultiplexer Circuits, Implementation of Boolean Functions using Decoder and Multiplexer, Arithmetic and Logic Units, BCD-To-Segment Decoder, Common Anode and Common Cathode, 7-Segment Displays, Random Access Memory, Read Only Memory and Erasable Programmable ROMs, Programmable Logic Arrays(PLA) and Programmable Array Logic (PAL)	**08**	**CO1, CO2**
III	**Introduction to Flip-Flops:** Basic Concepts of Sequential Circuits, Cross Coupled SR Flip-Flop Using NAND or NOR Gates, JK Flip-Flop Rise Conditions, Clocked Flip-flops, D-Types and Toggle Flip-flops, Truth Tables and Excitation Tables for Flip-flop. Master Slave Configuration Edge Triggered and Level Triggered Flip-flop, Elimination of Switch Bounce using Flip-flop, Flip-flop with Pre-set and Clear.	**10**	**CO2, CO3**
IV	**Sequential Logic Circuit Design:** Introduction to State Machine, Mealy and Moore Model, State Machine Notation, State Diagram, State Table, Transition Table, Table Excitation, Table and Equation, Basic Concepts of Counters and Register, Binary Counters, BCD Counters, Up Down Counter, Johnson Counter, Module-N Counter, Design of Counter using State Diagrams and Tables, Sequence Generators, Shift Left and Right Register, Registers with Parallel Load, Serial -in-Parallel-Out(SIPO) and Parallel-In-Serial-Out(PISO), Register Using Different Types of Flip-flops Designing synchronous circuits like Pulse train generator, Pseudo Random Binary Sequence generator, Clock generation.	**10**	**CO3**
V	**VLSI Design flow:** Design entry: Schematic, FSM & HDL, different modelling styles in VHDL/Verilog, Data types and objects, Dataflow, Behavioural and Structural Modelling, Synthesis and Simulation VHDL/Verilog constructs and codes for combinational and sequential circuit.	**07**	**CO3, CO4**
	Total Hours	**48**	

Essential Readings

1. Mano Morris, Digital Logic and Computer Design, Pearson Education, 14th ed. 2012.
2. A. Anand Kumar Fundamentals of Digital Circuits Prentice Hall India Learning, 4th ed. 2016.
3. D.V. Hall, "Digital Circuits and Systems", Tata McGraw Hill, 1st ed., 1989.
4. Charles Roth, "Digital System Design using VHDL", Tata McGraw Hill, 2nd edition, 2012.

Supplementary Readings

1. Brown S. and Zvonko Vranesic, Fundamental of Logic with Verilog Design, Tata McGraw Hill, 3rd Edition, 2013.
2. Kime Charies R and Morris Mano, Logic and Computer Design Fundamentals, Pearson Education, 4th Edition, 2013.