Logic Design of Quantum Circuits and Memristor-based Systems

OBJECTIVES

The primary objectives of the course are to expose the participants in the following:

a) Evolution of logic design paradigm over the years, and emerging technologies like quantum circuits and memristors.
b) Design and optimization of quantum circuits for logic design applications.
c) Physical architectures and constraints in the design of quantum circuits, and the corresponding technology mapping.
d) Working principles of memristors and their use in logic design and neuromorphic computing applications.

SPEAKERS

Prof. Bhargab B. Bhattacharya is a Professor of Computer Science and Engineering in the Advanced Computing and Microelectronics Unit, Indian Statistical Institute Calcutta. His research interests include VLSI design and test, VLSI physical design, nanotechnology and giga-scale integration.

Prof. Robert Wille is a Full Professor in the Institute for Integrated Circuits, Johannes Kepler University Linz, Austria. His research interests include reversible and quantum computing, and development of design technologies with particular focus on the design, verification and test of circuits and systems, for both conventional and emerging technologies.

Dr. KamalikaDatta is an Assistant Professor in the Department of Computer Science and Engineering, National Institute of Technology Meghalaya. Her research interest include reversible and quantum circuit synthesis and optimization, memristors-based system design, and embedded systems.

SCHEDULE

Module A: Introductory Module

Speaker: Bhargab B. Bhattacharya

Lecture 1: (Aug 08, 9:30-10:30 & 10:45-11:45) -- 2 hours

Evolution of logic design techniques over the years (conventional approach, binary decision diagram, Multiplexer based synthesis)

Lecture 2: (Aug 08, 14:00-15:00& 15:15-16:15) -- 2 hours

Other non-conventional logic design methodologies (Reed-Muller canonical form, exclusive-OR sum of Products form, threshold logic)

Module B: Logic design using Memristor

Speaker: Dr. Kamalika Datta

Lecture 3: (Aug 09, 9:30-10:30) -- 1 hour

Introduction to Memristor, principle of operation, memristor simulation models, memristor fabrication

Lecture 4: (Aug 09, 10:45-11:45 & 14: 00-15: 00) -- 2 hours

Logic design techniques using memristors, implementing IMPLY function using memristors, synthesis of logic functions using IMPLY functions

Lecture 5: (Aug 10, 9:30-10:30) -- 1 hour

Memristor crossbar array, issues and sneak path avoidance, using memristors to build threshold logic gates, applications to neuromorphic computing

Module C: Quantum circuits and their design

Speaker: Prof. Robert Wille

Lecture 6: (Aug 10, 10:45-11:45 & 12: 00-13: 00) -- 2 hours

Basics: Quantum circuits, reversible circuits, and their applications

Lecture 7: (Aug 11, 9:30-10:30) -- 1 hour
Design of reversible circuits (Synthesis and Verification)

Lecture 8: (Aug 11, 10:45-11:45) -- 1 hour
Design of quantum circuits (Decomposition and Optimization)

Lecture 9: (Aug 12, 9:30-10:30 & 10: 45-11: 45) -- 2 hour
Physical architectures and constraints (1D/2D quantum circuits, Nearest neighbour constraints)

Lecture 10: (Aug 12, 12: 00-13: 00) -- 1 hour
Demonstration of decomposition, mapping and optimisation tools

Mid Term Test: Aug 10, 15:00-16:00

End Term Test: Aug 12, 15:00-17:00

Note: Lecture notes will be provided; hands on session will be carried out using Revkit, ABC tool and SPICE

REGISTRATION & PAYMENT DETAILS

The registration fees for attending the course is as follows:

Industry/ Research Organizations: Rs. 10000
Academic Institutions: Rs. 5000
Student : Rs. 2500

Please register using the following link:
http://www.gian.iitkgp.ac.in/GREGN/index

Select our course and make payment using the following details:

Payment Mode: NEFT/RTGS/Fund Transfer

A/C no: NITMEG First name of the applicant Date of Birth (DDMMYY)GIAN
For Example: If an applicant's name is Anup Ghosh and date of birth is 12-06-1984. Beneficiary account number will be : NITMEGANUP120684GIAN

Beneficiary Name	**:**	**NIT Meghalaya fee account**
IFSC Code	**:**	**HDFC0000240**
Branch Name	**:**	**Sandoz Branch**
Last date of Registration:		**31st July, 2016**